AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method of forming a gate electrode in a semiconductor, comprising:

forming a first polysilicon film for the floating gate electrode on a semiconductor substrate and a dielectric film on the first polysilicon film;

forming a second polysilicon film for the control gate electrode on the dielectric film and a tungsten silicide film ~~sequentially on a semiconductor substrate~~ on the second polysilicon film;

performing an annealing process to crystallize the tungsten silicide film; ~~and~~

performing ~~an~~ a first etching process to etch the crystallized tungsten silicide film and the second polysilicon film under the crystallized tungsten silicide film at one time using the same etching gas after the annealing process; and,

performing a second etching process to etch the first polysilicon film for the floating gate electrode on a semiconductor substrate and the dielectric film on the first polysilicon film, thereby forming a gate electrode ~~comprising the tungsten silicide film and the polysilicon film~~.

2. (Previously Presented) The method of forming a gate electrode in a semiconductor according to claim 1, wherein the annealing process is one of a rapid thermal process (RTP) annealing process and a furnace annealing process for crystallizing an amorphous tungsten silicide film to form a crystalline tungsten silicide film.

3. (Previously Presented) The method of forming a gate electrode in a semiconductor according to claim 2, comprising performing the RTP annealing process at a temperature ranging from about 900°C to about 1000°C for a time period ranging from about

10 seconds to about 30 seconds in an ambient atmosphere of N_2 or NH_3 gas, and performing the furnace annealing process at a temperature ranging from about 850°C to about 1000°C for a time period ranging from about 5 minutes to about 30 minutes in an ambient of N_2 or NH_3 gas.

4. (Canceled)

5. (Currently Amended) The method of forming a gate electrode in a semiconductor according to claim 1, comprising performing the first etching process under a process condition for etching the second polysilicon film for the control gate electrode.

6. (Previously Presented) The method of forming a gate electrode in a semiconductor according to claim 5, wherein the first etching process is a dry etching process, and comprising performing the first etching process in an inductively coupled plasma chamber into which a mixture gas of Cl_2 gas and O_2 gas is introduced.

7. (Previously Presented) The method of forming a gate electrode in a semiconductor according to claim 1, wherein the first etching process is a dry etching process, and comprising performing the first etching process in an inductively coupled plasma chamber into which a mixture gas of Cl_2 gas and O_2 gas is introduced.

8. (Currently Amended) The method of forming a gate electrode in a semiconductor according to claim 1, where in the annealing process results in the etch rate of the crystallized metal silicide film being similar to that of the second polysilicon film for the control gate electrode.

9. (Previously Presented) The method of forming a gate electrode in a semiconductor according to claim 1, comprising forming the tungsten silicide film by reacting SiH_4 or SiH_2Cl_2 with WF_6 at a stochiometric ratio of (SiH_4 or SiH_2Cl_2): WF_6 of 2.0 - 2.8.